maintained at the state in which the data of "0" is latched by the input of the power-up reset signal PURST. Thereafter, the data "10011000" outputted from the flip-flops F1 through F8 are inputted to the NOR gates N1 through N8 of the control circuit for generating high voltage 3 respectively, and the output data "1001100" of the data input buffer is inputted to the inverters I1 and I8, respectively.

At this time, signals at a low level are outputted from only the output terminals VCVPB1 and VCVPB5 of the NAND gates NG2 and NG6 by the power-up reset signal PURST inputted with a low level and the program state signal PGM1 inputted with a high level. Therefore, a programming bias voltage is again applied to only the memory cells which are corresponded to the second and the sixth bits, respectively.

As mentioned above, the program circuit according to the present invention can apply a program voltage to only the memory cells which are not programmed during a re-programming operation. Therefore, the present invention can be prevent a lowering of reliability of the memory cell due to a continued supply of a program bias voltage.

The foregoing description, although described in its preferred embodiments with a certain degree of particularity, is only illustrative of the principle of the present invention. It is to be understood that the present invention is not to be limited to the preferred embodiment disclosed and illustrated herein. Accordingly, all expedient variations that may be made within the scope and spirit of the present invention are to be encompassed as further embodiments of the present invention.

What is claimed is:

1. A program circuit comprising:

a comparator for comparing output data of a data input buffer with output data of a sense amplifier bit by bit, and for outputting a re-program operation signal if the data are different from each other;

a data latch circuit for latching the comparing results of the output data of said data input buffer and the output data of said sense amplifier;

a control circuit for generating a high voltage for receiving the output data of said data input buffer and the data latched at said data latch circuit, respectively, and for outputting a signal for applying a program bias voltage to a memory cell which has not been completely programmed in response to a power-up reset signal and program state signal.

2. The program circuit as claimed in claim 1, wherein said comparator includes a plurality of exclusive-NOR gates to which output data of said data input buffer and output data of said sense amplifier, respectively, and a NOR gate for logically combining the output signals of said exclusive-NOR gates.

3. The program circuit as claimed in claim 1, wherein said data latch circuit includes a plurality of flip-flops, each flip-flop having a data input terminal to which comparing results of the output data of said data input buffer and the output data of said sense amplifier, a clock signal input terminal to which a program state signal and a reset signal input signal to which power-up reset signal/program state signal/read mode signals are inputted.

4. The program circuit as claimed in claim 1, wherein said control circuit for generating a high voltage includes a plurality of NOR gates to which output data of said data latch circuit and a power-up reset signal are inputted, respectively; a plurality of inverters to which output data of said data input buffer is inputted; and a plurality of NAND gates to which the output signals of said NOR gates, the output signals of said inverters and the program state signal are inputted, respectively.

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